

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tu Attorney Docket: TSM03-0188
Filed: Herewith Examiner: TBD
Serial No.: TBD Art Unit: TBD
For: Self-Aligned MIM Capacitor Process for Embedded DRAM

Mail Stop: Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form SB-08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Cite numbers 1-2 are newly cited prior art being filed under the waived requirement of 37 CFR 1.98 (a)(2)(i) dated July 11, 2003, therefore, copies of these U.S. patents are not included.

Respectfully submitted,

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